

SAMPLE RATE ADAPTION IN SIGNAL PROCESSING

The invention relates to the field of signal processing, particularly in communications systems.

From the perspective of signal reception, a mobile telephone typically comprises an antenna for receiving wireless signals transmitted to the telephone, a radio section for processing signals received on the antenna (e.g. amplification, frequency-conversion) and a digital section for manipulating the signals that are supplied by the radio section in order to recover information (such as speech) contained in the signals received on the antenna. Since the radio and digital sections operate on analogue and digital signals respectively, a mixed-signal section is provided between them. The mixed-signal section performs analogue to digital conversion (ADC) of the signals supplied by the radio section and conditions the resulting digital signals to render them suitable for processing by the digital section of the mobile telephone.

The manner in which a wireless telecommunications network operates depends upon the technical standard under which the network has been designed to operate. That is to say, there are a number of technical standards, each setting out a different scheme for operating a wireless telecommunications network. Examples of such technical standards are GSM, AMPS, CDMAOne and UMTS. Thus, it follows that the functionality of a mobile telephone will be dictated, to a large extent, by the technical standard for which it is intended. It also follows that a mobile telephone can only operate in a geographical location provided with coverage by a telecommunications network that is aligned to the same technical standard as the mobile telephone, thus restricting the likelihood that the telephone will be able to connect to establish a call.

One object of the invention is to provide a receiver architecture (such as may be incorporated in, for example, a mobile telephone) which is more likely to be able to establish a connection in a given location.

According to one aspect, the invention provides apparatus for preparing a signal, which has been received at a wireless communications device, to be processed by a receiver which will attempt to recover information conveyed by the signal, the apparatus comprising filtering means for filtering the signal in a digital form having samples appearing at a sample rate and adaption means for adjusting the sample rate, wherein the filtering means is capable of filtering the signal in a first manner which is required when the receiver is of a first type and in a second manner which is required when the receiver is of a second type, the adaption means is arranged to perform adjustments to the sample rate when the receiver is of the second and not the first type and the adjustments comprise altering the sample rate before the signal is filtered to permit the filtering means to perform filtering in the second manner and altering the sample rate after the signal has been filtered to provide the signal with a sample rate required by the second type of receiver.

The invention also consists in a method of preparing a signal, which has been received at a wireless-communications device, to be processed by a receiver which will attempt to recover information conveyed by the signal, the method comprising filtering the signal in a digital form having samples appearing at a sample rate using a filtering means capable of filtering the signal in a first manner when the receiver is of a first type and in a second manner when the receiver is of a second type and making sample rate adjustments to the signal when filtering is to be performed in the second manner but not when filtering is to be performed in the first manner, wherein said adjustments comprise adjusting the sample rate before the signal is filtered to permit the filtering means to perform filtering in the second manner and adjusting the sample rate after the signal has been filtered to provide the signal with a sample rate required by the second type of receiver.

Thus, the invention provides a processing stage that can interface with receivers of different types, meaning that a participant for a wireless communications network (e.g. a mobile telephone or a base station) can incorporate the processing stage according to the invention, leading to the design of a network participant that has the flexibility to use more than one type of receiver architecture to establish a call.

The processing scheme according to the invention is capable of operating on received communications signals formatted for the first and second receiver types. Typically, receivers of different types will require different sample rates for the processing of received communications signals in the digital domain. A receiver architecture will employ a crystal oscillator for providing a clock signal to control the sampling rate used for analogue to digital conversion of the received communications signals and it follows that different receiver architectures will require crystals operating at different frequencies. By adapting the sample rate of the output of the filtering means, the sample rate can be set to rates required by different receiver architectures without the need to provide a crystal oscillator specifically for each receiver architecture.

When conditioning signals for a receiver of the first type, the filtering process performs a first type of filtering and when conditioning signals for a receiver of the second type, the filtering process performs a second type of filtering. A single filtering means of an adjustable nature can be used to carry out the filtering, thus providing the advantage that the preparation of the signal for the receiver can be performed without requiring individual filtering means for the first and second receiver types.

In a preferred embodiment, the filtering of the signal is performed using an FIR filter arranged such that its tap coefficients are adjusted when switching operation between the types of receiver.

In a preferred embodiment, when signals are being conditioned for a receiver of the second type and the sample rate of the signal is being manipulated in advance of and following the filtering means, the filtering performed by the filtering means can be designed to eliminate errors arising from the manipulation of the sample rate.

Other signal processing operations can be performed on the signals within the invention as they pass between different parts of the signal processing scheme. For example, the signal to be supplied to the filtering process can be first be subjected to a correction for reducing any DC offset in the signal.

In one embodiment, the first type of receiver is a receiver operating according to a 3G telecommunications standard (e.g. UMTS) and comprising a rake receiver and the second type of receiver is a receiver operating according to a 2G telecommunications standard (e.g. GPRS) and comprising an equaliser.

By way of example only, an embodiment of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a mixed-signal chip;

Figure 2 is a block diagram of the chip of Figure 1 operating in a 3G mode;

Figure 3 is a block diagram of the chip of Figure 1 operating in a 2G mode; and

Figure 4 is a block diagram of a mobile telephone incorporating the chip of Figure 1.

The mixed signal chip 10 of Figure 1 receives signals from a radio section of a receiver architecture and conditions them for processing by a digital section of the receiver architecture (see Figure 4, discussed later). Such a receiver architecture can be used in, for example, a basestation or a subscriber unit of a wireless telecommunications network. The chip 10 is designed to process received radio signals of both the UMTS standard (denoted 3G for "Third Generation" in the figures) and the GSM standard (denoted to 2G for "Second Generation" in the figures). When operating with GSM radio signals, the chip 10 outputs digital signals conditioned for use by an equaliser in a digital signal processor (DSP) forming part of a digital processing section of a receiver architecture containing chip 10. When operating with UMTS radio signals, the chip 10 outputs digital signals conditioned for use by a rake implemented in hardware and forming part of a digital processing section of a receiver architecture containing the chip 10.

It should be noted that Figures 1 to 3 illustrate only the main blocks of the mixed-signal processing stage and a reader skilled in this art will appreciate that additional signal

processing operations can be performed on or with the signals present in or used by the chip 10.

Chip 10 operates with an input in the form of a GSM radio signal or a UMTS input signal, these alternatives being indicated by switch 12. Signals supplied from the radio section of the receiver architecture enter the chip 10 and are supplied to analogue to digital converter (ADC) 16 having an overall dynamic range of 8 bits.

The output of ADC 16 is supplied to a second order decimator 18. The decimator 18 operates to reduce the sample rate of the output of ADC 16. However, the decimator 18 only operates when the chip 10 is working with GSM signals. Otherwise, when the chip 10 is working with UMTS signals, the decimator 18 is inactive. The selective operation of decimator 18 is indicated diagrammatically by switch 20 which is closed when the chip 10 operates with UMTS signals and is open when the chip 10 operates with GSM signals.

After decimator 18, which may or may not be active, the output of the ADC 16 is supplied to DC correction unit 22. Correction unit 22 functions to reduce any DC offset error present in the digital signal (e.g. due to frequency conversion in a radio section of a receiver architecture providing the radio signals received by the chip 10). The manner in which such a correction unit may be implemented is well known. From the correction unit 22, the digital signal passes to a 33-tap FIR digital filter 24. The output of the filter 24 can then follow one of two paths 26, 28.

Path 26 allows the digital signal representing the radio signals supplied to the chip 10 to be supplied to a DSP in a digital section of a receiver architecture and implementing an equaliser. Path 28 allows the digital signal representing the radio signals supplied to the chip 10 to be supplied to a rake forming part of the digital processing section of the receiver architecture. Path 26 includes a sample rate adaption unit 30 for adjusting the sample rate of the digital signal travelling on path 26 to the rate required for the equaliser. Adaption unit 30 comprises a first order interpolator 32 and a second order decimator 34. The interpolator 32 adds samples into the digital signal travelling on path 26 and decimator 34 removes samples from the signals travelling on path 26. By choosing appropriately the

factors by which the interpolator 32 and the decimator 34 increase and decrease respectively the sample rate of the signal travelling along path 26, the sample rate of the signal supplied to the DSP can be set.

The operation of chip 10 with UMTS signals and GSM signals will now be described with reference to Figures 2 and 3 respectively.

In Figure 2, only the main elements of chip 10 that are used in the processing of UMTS signals from a radio section of a receiver architecture are shown. For example, decimator 18 is not shown in Figure 2. Elements in Figure 2 that have already been described with reference to the Figure 1 retain the same reference numerals.

In order to process UMTS signals, the mixed-signal chip 10 requires an ADC with a 6 bit dynamic range sampling at a rate of 19.2MHz. As shown in Figure 2, a clock signal at 19.2MHz is supplied along path 36 and is used to control the operation of ADC 16 and filter 24. The clock signal at 19.2MHz is derived by multiplying by a factor of 5 the frequency of a 3.84MHz crystal oscillator located in the unit (e.g. mobile telephone) containing the chip 10. To satisfy the processing requirements for UMTS signals, the ADC 16 uses the 6 least significant bits of its dynamic range to output a 6 bit digital signal.

The ADC 16 outputs a signal at a sample rate of 19.2MHz. This signal undergoes DC offset correction at correction unit 22 and then passes to the FIR filter 24. The taps of the FIR filter are programmed to implement a Raised Root Cosine response in order to meet the requirements of the UMTS standard. The filter may also be programmed to compensate for frequency distortions introduced by the radio section of the receiver architecture. The output of the filter is then passed from the chip 10 to a rake in a digital section of a receiver architecture where it is prepared for subsequent processing in the digital section (e.g. to ultimately recover speech information).

In Figure 3, only the main elements of the chip 10 that are used in the processing of GSM signals from a radio section of a receiver architecture are shown. Elements in Figure 3 that have already been described with reference to Figure 1 retain the same reference numerals

and their function will not be described again in so far as their function was described with reference to Figure 2 and still remains the same in the GSM operating mode.

In order to process GSM signals, the mixed-signal chip 10 uses the same 19.2MHz clock signal that is used for UMTS operation. The 19.2MHz clock signal is supplied along path 38. The 19.2MHz clock signal is passed to a clock divider 40 which halves the rate of the clock signal to 9.6MHz. The 9.6MHz clock signal is used to clock the ADC 16 and the second order decimator 18. Therefore, the ADC outputs a digital signal with a sample rate of 9600 ksps ("kilo" samples per second). The output of the ADC 16 is supplied to the decimator 18 which performs a factor of 12 reduction in the sample rate of the output of the ADC 16. Therefore, the output of the decimator 18 has a sample rate of 800 ksps. The output of the second order decimator 18 undergoes DC offset correction at correction unit 22 and is then supplied to the FIR filter 24.

Since the input to the filter 24 has a sample rate of 800 ksps, the signal used to clock the filter needs to have a rate of 800kHz. The clock signal for the filter is supplied by a clock divider 42 operating on the 9.6MHz clock signal provided by clock divider 40. Clock divider 42 reduces the 9.6MHz clock signal by a factor of 12 to produce a clock signal at the rate of 800kHz required by filter 24. When operating in the GSM mode, the tap coefficients of the filter 24 are chosen to provide an optimal fit for a normal GSM filter, taking into account the frequency spectrum errors introduced by the decimator 18 and the adaption unit 30. That is, the filter coefficients are chosen to correct for any frequency distortion of the spectrum caused by decimator 18 and to provide an advance correction for any distortion of the frequency spectrum that will be caused downstream by the adaption unit 30. The filter may also be programmed to compensate for frequency distortions introduced by the radio section of the receiver architecture.

The adaption unit 30 uses a combination of interpolation and decimation to allow the output of filter 24 to attain a sample rate of 270.83ksps as required by a GSM equaliser. Within adaption unit 30, the output of the filter 24 is first interpolated to increase the sample rate by a factor of 65 (at 32) and is then decimated (at 34) to reduce the sample rate by a factor of 192. The net effect of the adaption unit 30 is to change the sample rate of the

output of filter 24 by a factor of $\frac{65}{192}$ the filter output with a sample rate of 270.83kps. The adaption unit 30 is not clocked using the signal supplied to path 38. The adaption unit is clocked by a clock signal supplied by the DSP and having a minimum clock frequency of 52MHz. On the assumption that the interpolator 32 can insert one sample value per clock cycle, 52MHz is the minimum clock frequency that will permit the 800kps output of the filter to be interpolated by a factor of 65.

In the embodiment of Figures 1, 2 and 3, a single clock signal of 19.2MHz is supplied to a mixed signal chip in order to produce GSM and UMTS outputs with sample rates of 270.83 and 19200kps respectively. Since the 19.2MHz clock signal is used in both GSM and UMTS modes, there is no need to provide different clock signals for each mode with the result that only a single crystal oscillator is required, generating a 19.2MHz signal. Moreover, the use of a reconfigurable filter (FIR filter 24) permits a single piece of filtering hardware to be used to perform the differing types of filtering required by UMTS and GSM.

The mixed signal chip 10 will typically form part of a receiver architecture, located within, for example, a mobile phone such as that shown in Figure 4. Figure 4 shows only the main elements of a mobile telephone as required for the reception of signals. Signals are received at antenna 44 and are processed in radio section 46. The resulting received radio signals then need to be processed in the digital domain by digital processing section 48 and are therefore conditioned appropriately by the mixed signal chip 10.